CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of forming an electrical contact to a silicon-containing substrate comprising the steps of:

(a) forming an alloy layer having the formula MX over a silicon-containing substrate, wherein M is a metal selected from the group consisting of Co and Ni and X is an alloying additive;

(b) annealing said alloy layer at a temperature sufficient to form a metal alloy silicide, MXSi, layer; and

(c) removing any remaining alloy layer.

2. The method of Claim 1 further comprising pre-annealing the alloy layer prior to step (b) at a temperature sufficient to form a metal rich alloy silicide, M_2XSi, layer.

3. The method of Claim 1 further comprising a second annealing step after step (c) which is conducted at a temperature that converts the MXSi layer into a metal alloy disilicide, $MXSi_2$, layer.

4. The method of Claim 1 further comprising forming an optional barrier layer over said alloy layer prior

to step (b), wherein said optional barrier layer is removed by step (c).

5. The method of Claim 1 wherein said alloying additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

6. The method of Claim 5 wherein said alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir or Pt.

7. The method of Claim 6 wherein said alloying additive is Si, Ti, V, Cr, Ni, Ge, Nb, Rh, Ta, Re or Ir.

8. The method of Claim 1 wherein said alloying additive is present is said alloy layer in an amount of from about 0.01 to about 50 atomic %.

9. The method of Claim 8 wherein said alloying additive is present is said alloy layer in an amount of from about 0.1 to about 20 atomic %.

10. The method of Claim 1 wherein M is said alloy layer comprises a Co alloy.

11. The method of Claim 4 wherein said optional oxygen barrier layer is composed of TiN.

12. The method of Claim 1 wherein said silicon-containing substrate comprises a single crystal Si, polycrystalline Si, SiGe, amorphous Si, or a silicon-on-insulator (SOI).

13. The method of Claim 1 wherein said alloy layer is comprised of a single phase.

14. The method of Claim 13 wherein said single phase is a face centered cubic phase.

15. The method of Claim 2 wherein said pre-annealing step is carried out using rapid thermal annealing (RTA).

16. The method of Claim 15 wherein said RTA is carried out at a temperature of from about 350° to about 450°C for a time period of from about 10 to about 300 seconds.

17. The method of Claim 1 wherein said annealing step (b) is carried out by RTA.

18. The method of Claim 17 wherein said RTA is carried out at a temperature of from about 400° to about 700°C for a time period of from about 10 to about 300 seconds.

19. The method of Claim 1 wherein said remaining alloy layer is removed utilizing a wet etch step that includes the use of an etchant that is selective for removing said layers.

20. The method of Claim 3 wherein said second annealing step is carried out by RTA.

21. The method of Claim 20 wherein said RTA is carried out at a temperature of from about 700° to about 900°C for a time period of from about 10 to about 300 seconds.

22. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material, said silicon-containing semiconductor material being doped with an impurity to provide carriers of holes, electrons or both holes and electrons; and

a first layer of $CoXSi_2$, wherein X is an alloying additive, said alloying additive being present in said first layer in an amount of from about 0.01 to about 50 atomic %,

said first layer and said silicon-containing semiconductor material forming an interface having a predetermined roughness and being substantially free of Co silicide spikes descending into said silicon-containing semiconductor material.

23. The electrical contact of Claim 22 wherein said alloying additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La,

Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

24. The electrical contact of Claim 23 wherein said alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir or Pt.

25. The electrical contact of Claim 24 wherein said alloying additive is Si, Ti, V, Cl, Ni, Ge, Nb, Rh, Ta, Re or Ir.

26. The electrical contact of Claim 22 wherein said alloying additive is present in said first layer in an amount of from about 0.1 to about 20 atomic %.

27. An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material, said silicon-containing semiconductor material being doped with an impurity to provide carriers of holes, electrons or both holes and electrons; and

a first layer of NiXSi, wherein X is an alloying additive, said alloying additive being present in said first layer in an amount of from about 0.01 to about 50 atomic %,

said first layer and said silicon-containing semiconductor material forming an interface having a predetermined roughness and being substantially free

of Ni silicide spikes descending into said silicon-containing semiconductor material.

28. The electrical contact of Claim 27 wherein said alloy additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

29. The electrical contact of Claim 28 wherein said alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir or Pt.

30. The electrical contact of Claim 29 wherein said alloying additive is Si, Ti, V, Cr, Ni, Ge, Nb, Rh, Ta, Re or Ir.

31. The electrical contact of Claim 27 wherein said alloying additive is present in said first layer in an amount of from about 0.1 to about 20 atomic %.

32. A method for the formation of a silicide phase in a silicon-containing substrate said method comprising at least a step of forming an alloy layer having the formula MX over said silicon-containing substrate, wherein M is a metal selected from the group consisting of Co and Ni and X is an alloying additive whereby said alloy layer controls the temperature of formation of various silicide phases.